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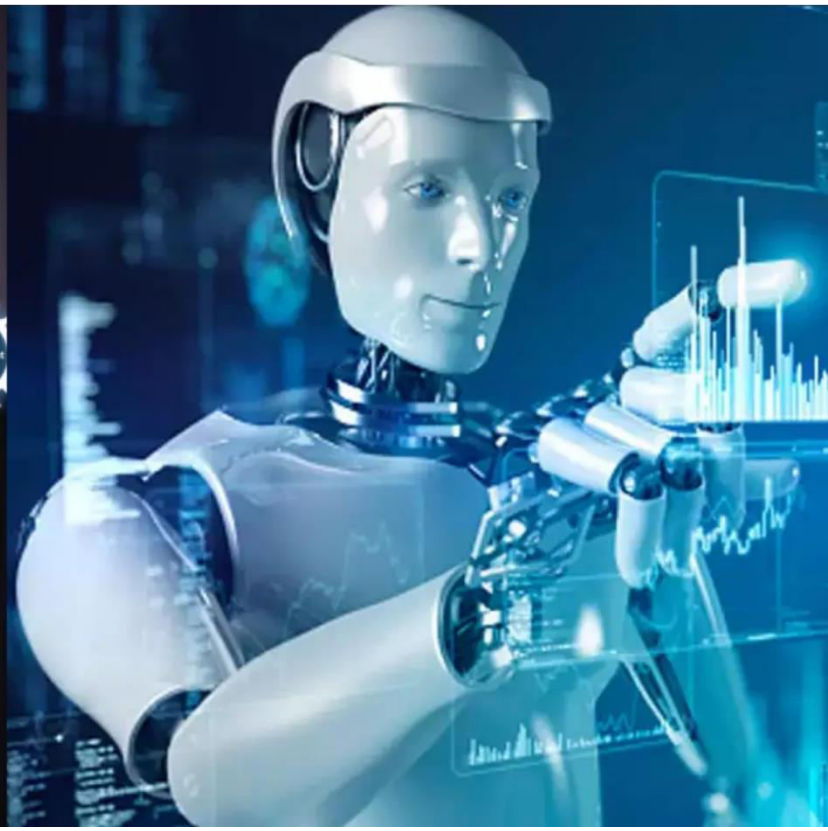
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Machine Learning-Driven Prediction of Optimal Design Parameters for Ripple Carry Adder

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ABSTRACT: The Ripple Carry Adder (RCA) is one of the most widely used arithmetic circuits in digital systems because of its simple architecture and low hardware cost. However, selecting optimal design parameters such as transistor sizing, supply voltage, propagation delay, power consumption, and area often requires multiple design iterations and extensive simulations, increasing the overall design time. To address this challenge, this work presents a Machine Learning (ML)-driven framework for predicting the optimal design parameters of a Ripple Carry Adder. A dataset is generated using circuit simulations under different design conditions, and relevant features are extracted to train supervised ML models. The trained model learns the relationship between input design parameters and performance metrics, enabling rapid prediction of optimized configurations without performing repeated simulations. The proposed approach significantly reduces design exploration time while maintaining high prediction accuracy for power, delay, and power-delay product (PDP). Experimental results demonstrate that the ML-based prediction model provides reliable optimization guidance, allowing designers to achieve efficient RCA implementations with reduced computational effort. This methodology offers a scalable and intelligent design automation solution for next-generation low-power and high-performance VLSI circuit design.

KEYWORDS: CMOS,delay, device dimension, power, prediction model, VLSI.

I. INTRODUCTION

In recent years, the rapid advancement of Very Large-Scale Integration (VLSI) technology has increased the demand for digital circuits that provide high performance, low power consumption, and reduced chip area. Arithmetic circuits are essential components of modern digital systems, including microprocessors, digital signal processors, embedded systems, and application-specific integrated circuits (ASICs). Among these circuits, adders are fundamental building blocks used to perform arithmetic operations such as addition, subtraction, address calculation, and data processing. Therefore, optimizing adder design parameters is an important step toward improving the overall efficiency of digital systems.

A Ripple Carry Adder (RCA) is a conventional binary adder architecture consisting of interconnected full-adder stages. In this architecture, the carry output of each stage is propagated to the next stage until the final carry is generated. A 3-bit Ripple Carry Adder adds two 3-bit binary operands along with an optional carry input to produce a 3-bit sum and a final carry output. Due to its simple structure, regular design, and relatively low hardware complexity, the ripple carry adder is widely used as a basic architecture for studying digital circuit design and optimization. However, the sequential propagation of carry signals introduces propagation delay, which can affect circuit performance. Consequently, optimizing the power consumption, propagation delay, and area of a ripple carry adder is essential for achieving efficient circuit operation.

The performance of a 3-bit Ripple Carry Adder is influenced by several design parameters, including transistor sizing, supply voltage, threshold voltage, and circuit implementation technology. These parameters directly or indirectly affect power dissipation, switching behavior, propagation delay, and silicon area. Conventional optimization techniques generally rely on repeated circuit simulations and manual parameter adjustments to identify suitable design configurations. Although these approaches can provide accurate results, they may require considerable simulation time and computational resources when exploring a large number of possible parameter combinations. Furthermore,

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optimizing one performance metric may negatively affect another, creating a trade-off among power, performance, and area (PPA).

Machine Learning (ML) offers a promising solution for addressing these optimization challenges by learning the relationship between circuit design parameters and their corresponding performance metrics. ML algorithms can be trained using datasets generated from circuit simulations or experimental measurements to predict circuit behavior for different design configurations. Once trained, these models can estimate important performance characteristics without requiring a complete circuit simulation for every parameter combination. This capability enables faster design-space exploration, reduces repetitive simulation effort, and supports data-driven decision-making during circuit optimization.
In this research, a machine learning-driven approach is proposed to predict optimal design parameters for a 3-bit Ripple Carry Adder. The proposed approach involves generating a dataset by varying selected design parameters and evaluating the resulting circuit performance using an appropriate simulation environment. The generated dataset is then used to train and evaluate machine learning models for predicting key performance metrics, such as propagation delay and power consumption, along with area when it can be reliably estimated. Based on the model predictions, suitable design parameter combinations are identified according to predefined optimization objectives. The predicted configurations can subsequently be validated through circuit-level simulations to determine the accuracy of the machine learning models and the effectiveness of the optimization process.

The main objective of this work is to investigate the feasibility of using machine learning to improve the efficiency of design-space exploration and identify suitable design parameters for a 3-bit Ripple Carry Adder. By combining circuit simulation with predictive modeling, the proposed approach aims to reduce dependence on repetitive simulations and provide an efficient framework for performance optimization. The methodology may also serve as a foundation for extending machine learning-based optimization to more complex arithmetic circuits and larger digital systems.

II. LITERATURE SURVEY

This research investigates the optimization of supply voltage and device dimension for a 2-bit RCA, considering average power consumption and worst-case delay parameters. The optimization challenge can be formulated as a supervised learning-based regression problem, since regression analysis serves two fundamental purposes in this context. First, it functions as a forecasting and prediction tool, and second, it enables the discovery of causal relationships between independent and dependent variables. The regression models quantify the predictive capability of independent variables concerning dependent variables. This study applies regression analysis to establish relationships between independent and dependent variables within the specified design parameters. A regression problem can be broadly classified into single-output regression and multi-output regression [14]. Single output regression can be further subdivided into (a) simple linear regression (b) multivariate regression, and (c) polynomial regression. Simple Linear regression defines the linear relationship between the dependent variable and the independent variable. Multivariate Regression is a statistical technique used to predict the outcome of a dependent variable, using a multiple explanatory variable. The prime objective is to model the linear relationship between independent variables and dependent variable. Polynomial regression is regression analysis that performs nth degree polynomial modeling of the relationship between independent and dependent variables. Polynomial regression is a special case of multivariate regression, where the polynomial equation allows for a curvilinear interplay of the dependent and independent variables. Multi-output regression enables simultaneous prediction of multiple real-valued targets. This approach addresses common challenges including missing data, noise, and complex dependencies between features and targets. The current study's requirements align with this machine learning framework, as it effectively models multi-input and multi-output datasets while considering both feature-target relationships and inter-target correlations, ensuring superior representation of complex problems. The authors in [4] presented a ML model to be integrated with VLSI design flow for predicting runtime for various VLSI design steps for enhanced resource management and scheduling as well. This will allow the designers to have a prior estimate of turnaround time to manage EDA tool usage for optimal workflow especially when iterative design steps are involved. Recent literature demonstrates significant advancements in machine learning applications for circuit design parameter prediction, particularly in power estimation and optimization. The study in [6] systematically evaluates decision trees, random forests, and artificial neural networks (ANNs) for power prediction accuracy and reports the random forest algorithm to achieve superior performance in terms of both mean squared error (MSE) and correlation coefficients, attributed to their ensemble learning approach and ability to handle non-linear relationships in circuit parameters. ANN is explored for predicting device parameters including the device currents, threshold voltage and sub-threshold swing in[9]and[10]based on environmental factors like temperature and other

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physical device parameters like channel length, doping levels and thickness. A graph learning-assisted neural network model (GLAAPE) is presented in [15] to capture the structural information of circuit designs. GLAAPE demonstrates remarkable efficiency in power estimation for gate-level combinational designs based on register transfer level (RTL)simulations withapproximately85%reductionin estimation time compared to conventional simulation-based methods while maintaining accuracy within 5% of detailed power analysis tools. Complementary research [5] presents a sophisticated ML-based regression framework specifically tailored for power consumption estimation in metal oxide semiconductor field effect transistor (MOSFET)-based digital circuits. The study develops a comprehensive dataset encompassing various circuit layouts, including P-type metal oxide semiconductor (MOS) and N-type MOS-based resistive load inverter and complementary MOS(CMOS)based nand gates. The methodology involves careful feature selection incorporating key electrical parameters such as threshold voltage variations, parasitic capacitances, and switching activities. The regression model demonstrates robust performance across different technology nodes and operating conditions, validating its applicability in practical design scenarios. Building upon these foundations, [6] presents a notable advancement in power estimation accuracy using random forest modeling. Their approach incorporates an extensive feature set including both static and dynamic power components, achieving remarkable precision with a root-mean square error (RMSE) of 0.00016 and R2 score of 0.99938. The methodology employs a sophisticated cross-validation strategy and hyper parameter optimization framework, ensuring model robustness across diverse circuit configurations. The study's significance lies in its practical applicability to real-world CMOS VLSI circuit design, demonstrating that machine learning techniques can achieve accuracy levels comparable to traditional simulation program with integrated circuit emphasis (SPICE) simulations while significantly reducing computational overhead. Five different regression approaches were compared in [16] including linear, decision tree, random forest, Gradient Boosting and Xtreme Gradient Boosting, for estimating dynamic power for digital VLSI circuits. The dataset comprised of features collected from synthesis report from 103digital circuits. The various features used for the study are number of logic elements, input and output pins, fanouts and power dissipation. The results showed that Xtreme Gradient boosting regressor gave the most accurate performance. Analog circuit designs have always required handling huge design space search and conflicting traded off constraints which provides a great opportunity for implementing ML methods for parameter prediction. Supervised and unsupervised learning methods are compared in [17] for analog circuit design optimization. A transconductance versus drain current approach is used for common source amplifiers and two-stage single-ended operational amplifiers to generate the data for training the ML model. Similarly, to reduce the time for simulating large number of circuits to generate data set, a polynomial equation based symbolic filter is used in [18] to model analog circuit sizing problem. The circuit performance is evaluated based on this symbolic analysis which uses curve-fitting results from the worked out small-signal parameter values and circuits satisfying the requirements for simulation. Moreover, the model combines reinforcement learning with deep learning to make the proposed model self-improving. This approach specifically addresses yield improvement by simultaneously optimizing leakage power and propagation delay constraints, demonstrating the potential of hybrid learning techniques in circuit design. Further, use of ML-based global offline surrogate models for different circuit parameters is validated in [19] with the study of band gap reference, folded cascode and two stage operational amplifier circuits. These models are used to validate the feasibility of a new design before invoking call for NG SPICE simulation to save simulation time by avoiding the need to develop accurate mathematical models of the circuit. ML is applied for determining the aspect ratio for MOS for a common source amplifier with diode connected load without the knowledge of NG SPICE technology parameters[20]. The size of the field effect transistor (FET) was predicted based on voltage gain, power dissipation, supply, and input impedance with best results obtained for neural network when compared with decision tree, general regression neural network (GRNN) and support vector regression. Current-voltage relationship is used to train neural networks for predicting optimized doping profile and design window of channel geometry for nano sheet FETs in [18] using a multi-objective optimization function based on current, on-off current ratio and threshold swing. The gap between the schematic and layout simulations is addressed with the help of ML-driven framework for predicting circuit performance metrics in [21]. The study is based on ring oscillators with different number of stages, supply voltages, temperature at different process corners. The work uses random forest regressor, neural networks and xtreme gradient boosting regressor to predict power and frequency metrics for the circuits with meanabsolutepercentageerroraslowas5%. Moreover, it is shown that with reduced technology nodes, neural networks and xtreme gradient boosting regressor perform better with far lesser number of simulations. Deep reinforcement learning is studied in [22] while treating VLSI design as equential Markov decision-making process. Design parameters, including supply voltage, clock frequency, clock and power gating, workload scheduling, and memory configurations are regulated to achieve lowest possible power consumption with optimal performance and thermal limitations. ML has also been employed for synthetic dataset generation in [23] for improved accuracy of the subsequent models with larger training datasets. The synthetic data generated is used to improve prediction accuracy of

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gradient-boosting regression model for delay of twelve different digital cells including gates, full adder and multiplexer. The gradient-boosting regression model, trained on synthetic data was validated against NGSPICE simulations and it is reportedly able to predict delay for these circuits with low error. The comprehensive review of literature reveals several key insights and research opportunities in the application of machine learning to VLSI circuit design optimization. The progression from simple regression models to sophisticated multi-output regression frameworks demonstrates the evolving complexity and capability of machine learning approaches in circuit design.

TABLE 1. Truth table for full adder.

a_1	b_1	c_0	Sum_1	$Cout_1$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

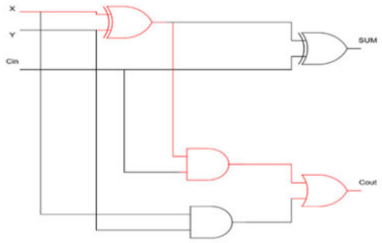


FIGURE 1. 1-bit full adder circuit.

The literature shows strength in power estimation techniques, with various studies achieving high accuracy through different machine learning architectures, from traditional random forests to advanced graph neural networks. While individual parameter optimization has been well-explored, there is a notable gap in approaches that simultaneously optimize multiple interdependent parameters. The existing multi-output regression frameworks, though theoretically capable,have not beenfully exploited in the context of VLSI circuit design optimization and parameter estimation. These observations establish the foundation for the current research, which aims to address these limitations by implementing a comprehensive multi-output regression framework for simultaneous optimization of supply voltage and transistor sizing in VLSI circuit design. This approach promises to capture the complex inter dependencies between multiple design parameters while maintaining computational efficiency.

III. METHODOLOGY

This work aims to predict three target variables—supply voltage, NMOS width and PMOS width—based on average power consumption and critical delay constraints of the circuit. Enabling accurate capture of target variable relationships will ensure reliable estimation.

A. CIRCUIT SELECTION

Adders are an integral part of almost every system; hence it is chosen as the circuit for this study. A 1-bit full adder circuit performs addition of the input bits a1, b1 with carry c0. The circuit diagram and truth table for 1-bit full adder are presented in Figure 1andTable1respectively. The full bit adders can be cascaded together such that carry-out of one stage is made the input of next, to form n-bit adders. Equations (1) and (2) provides the Boolean expression for output sum and carry (cout) of nth bit full adder with the circuit shown in Figure 1.

$$sum_n = a_n \oplus b_n \oplus c_{n-1} \quad (1)$$

$$carry_{out} = a_n * c_{n-1} + b_n * c_{n-1} + a_n * b_n \quad (2)$$

(1) (2) This paper implements a 3-bit RCA using two 1-bit full adders in cascade as shown in Figure 2. The output carry of the first full adder is given as carry-in for the second, creating the ‘‘ripple’’ effect, hence the name RCA. The three-bit inputs are (A0,A1, A2) and (B0,B1, B2) respectively with input carry bit represented as C0. The output is generated as a 3-bit sum represented as (S0,S1, S2) and a carry bit C2 and C3. The 3-bit adder from our previous work [20] is utilized for NGSPICE simulation. The input-output waveforms for 3-bit RCA implementation are shown in Figure3.Average power and delay were calculated for various combinations of supply voltage, PMOS/NMOS widths for dataset-generation for this paper.

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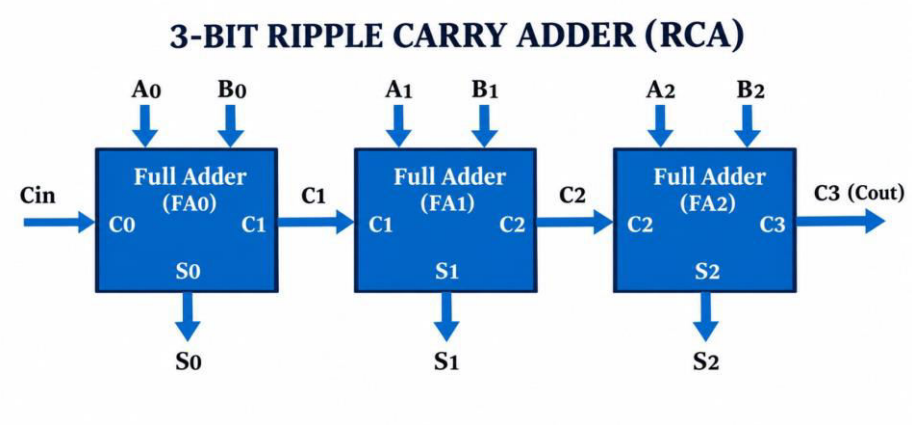


FIGURE.2. 3-bit RCA using the 1-bit full adders

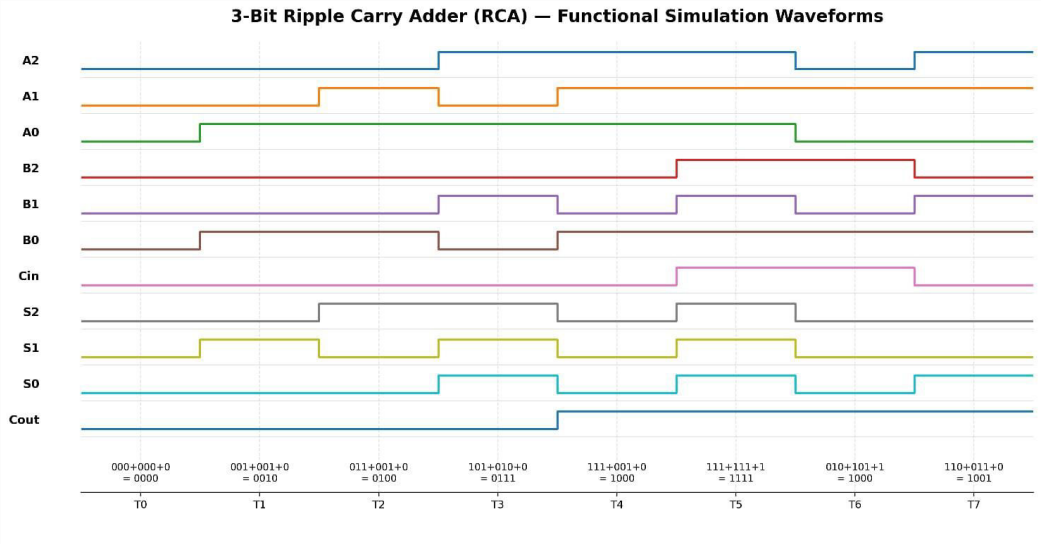


FIGURE.3. Demonstration of signals a0, a1, a3,b0, b1,b2 cin, sum0, sum1,sum2, carryout.

B. DATASET CREATION

The steps for complete workflow from the automated NGSPICE simulations,through Pythonscript-driven parameter looping and data extraction, to the final stage of ML model training and prediction is shown in Figure 4. Each stage of this workflow, along with its underlying objective, is detailed in subsequent sections. The dataset was created for various combinations of supply voltage with the NMOS and PMOS device dimensions. The range of variation in supply voltage, NMOS width, and PMOS width is summarized in Table 2. The dataset consists of 8000 data points, with 80% data allocated for model training, and the remaining 20% for testing and validation purposes after removing the outliers. The delay considered for the work is the worst-case delay of an adder circuit, corresponding to the longest path i.e. from input a0 to the cout. As shown in Figure 1, choosing this critical path delay ensures the robustness of the dataset. For average power calculation, the input signals were considered such that it takes all possible combinations that a 2-bit adder can encounter.

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TABLE 2. Parameter range for dataset creation.

Simulation Input Parameters	Range
V_{dd} and V_{in}	0.9 V - 2.5 V
NMOS Width	128 nm - 441.6 nm
PMOS Width	300 nm - 1035 nm

An excerpt of the dataset used for training the machine learning model is demonstrated in Table 3.

TABLE 3. Sample training dataset.

Supply (V)	PMOS width (nm)	NOS width (nm)	Average power (W)	Delay (s)
0.9	300	128	410.4131p	376.5445p
0.9	315	134.4	529.6088p	377.3519p
0.9	330	140.8	664.3193p	376.7275p
0.9	345	147.2	812.9895p	367.3688p
0.9	360	153.6	973.8639p	374.0197p
0.9	375	160	1.1451n	377.3235p
0.9	390	166.4	1.3249n	378.7885p
0.9	405	172.8	1.5114n	373.9601p
0.9	420	179.2	1.7030n	365.9836p

Once the SPICE netlist is generated, the next step involved automating the process of updating the netlist and performing repeated simulations across the defined range of parameters. This automation was achieved through Python scripting. A list of defined parametric values was created, and the simulation was looped over these values. The detailed steps involved in extracting required data from the simulation are outlined below:

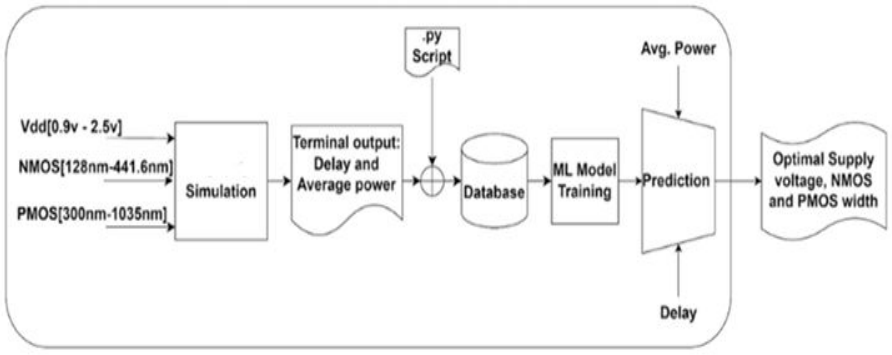


FIGURE 4. Simulation to prediction workflow.

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1. A list of parametric values across a defined range was generated, and the original NGSPICE netlist was updated iteratively. Each iteration simulated specific values of the parameters using the sub process. POPEN() python method, and the output was stored in a.txt file.
2. The simulation outputs, specifically average power, and worst-case delay were extracted from the respective.txt files and added to a.csv file, thereby completing the dataset creation.

C. DATA PREPROCESSING

Effective data preprocessing is significant in ensuring the quality and consistency of input data for ML models. In this work, data preprocessing is carried out with a pipelined approach to effectively handle variations in measurement units, scale the data appropriately, and identify the best fitting model in accordance with correlation between variables. The following steps outline the stages involved in the data preprocessing using pipeline:

1. Unit Conversion: This step ensures consistency across the dataset by removing any missing values and assigning a standard measuring unit to all data points. Here, data points were converted into nanoseconds (ns) and nanowatt(nW) scales,preparing the model to be trained for delay in nanoseconds and power in nanowatts.

2. Data Normalization: As shown in Table 3, the dataset exhibits high variance due to the presence of features with differing physical units and magnitude. To mitigate the risk of outliers skewing the transformation, the training database is constrained within the 75th to 25th percentiles. This ensures that the target parameters (power, delay) and features (transistor widths, and supply voltage) are free from extreme outliers. The min and max values used for scaling were therefore representative of the true operational range of our circuits. In the absence of such outliers, min-max scaling is a safe and effective linear transformation. Further, data normalization is applied which rescales all the data points to [0,1] range. This process improves the convergence rate of the model and reduces variance, enhancing stability during training.

3. Parameter Interdependence Analysis: Combinations of input parameters are plotted against output parameters to observe trends and correlations, helping to decide the ML model to implement. The results of these plots are discussed below.

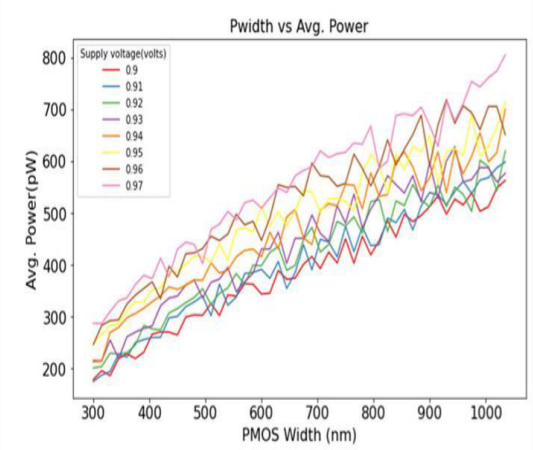


FIGURE 5. PMOS width vs power.

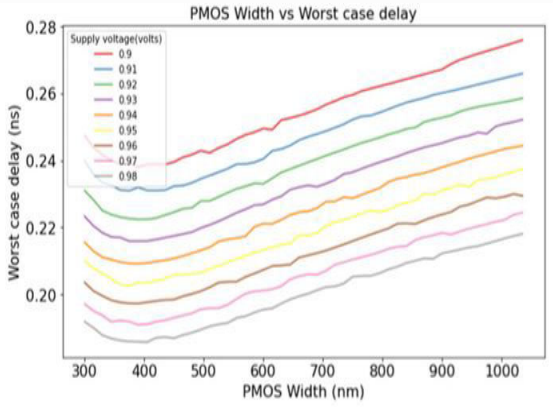


FIGURE 6. Worst case delay and PMOS width.

The plot in Figure 5 indicates a gradual linear increase in average power as the PMOS width increases. Similarly, an increasing trend across supply voltage and average power is observed. Similarly, worst case delay also exhibits a linearly increasing trend with PMOS width, as shown by the plot in Figure 6. Since the ratio between PMOS and NMOS widths remains constant at 2.34 throughout the dataset, a similar relationship holds for NMOS width. Figure 7 highlights an exponentially decreasing relationship between worst case delay with increasing supply voltage whereas an exponentially increasing relationship is observed for average power as shown in Figure 8. Based on the trends and patterns identified between parameters, a multi-output regression model was selected for predicting the target variables.

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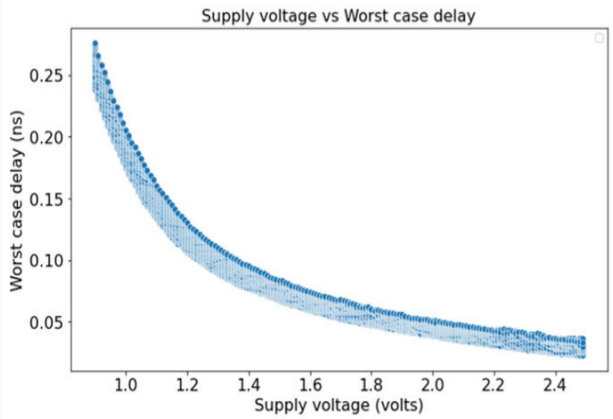


FIGURE 7. Supply voltage vs worst case delay.

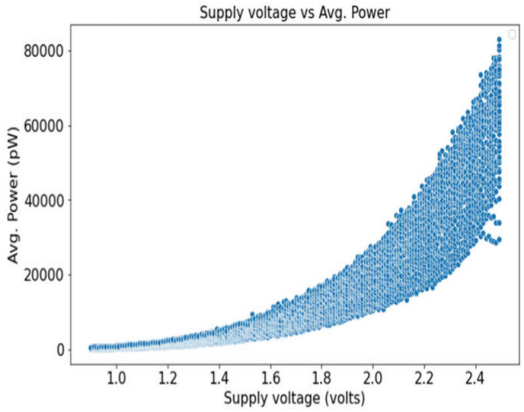


FIGURE 8. Supply voltage vs power.

D. MODEL SELECTION AND TRAINING

A multi-output regressor model is particularly suited to real-world problems involving multiple target prediction, especially when the variables have interdependency. When prediction of one variable influences the prediction of another, this model proves effective. This makes multi-output regressor model ideal for addressing the parameter interdependence observed in the dataset. The average power and worst-case delay are considered as input to ML model which targets to predict supply voltage, NMOS width and PMOS width. The problem is formulated with a cascaded prediction mechanism, that is, by incorporating the initial prediction of supply voltage recursively as an input feature for subsequent prediction of transistor widths. Adirect benchmark is difficult due to the strong dependency of design parameters under consideration on technology node, circuit design, transistor type and EDA tools. Hence, the strength of this work is demonstrated through validation performed on the SPICE simulation results which acts as golden baseline. The problem at hand is configured as multi-output with a cascaded prediction mechanism. In this architecture, the initial prediction for supply voltage is recursively used as features to perform subsequent predictions for optimal device width, NMOS width and PMOS width, thereby more accurately modeling the inter-target relationship. As a method to check for reliability of our model, linear regression with regularization is compared with other state-of-the-art ML models like polynomial regression and artificial neural networks. Polynomial regression is analyzed across 5-10 degrees and artificial neural networks is analyzed for upto10 hidden layer architecture. The comparative performance of these models under consideration is shown in Table 4. These models are evaluated based on standard performance metrics such as R2 score and MSE defined in equation (3) and (4) respectively. The R2 score as well as mean absolute error (MAE) ranges between [0,1]. The value of R2 score closer to 1 indicates better fit of the model with the data and hence better accuracy in prediction. The same is true if the value of MSE is closer

TABLE 4. Comparison of different ML models for considered circuit configuration.

Model	R^2 Score	MAE
Multi-target Linear Regressor	0.98	11.37
Polynomial Regression (Degree 6)	0.81	0.00022
Polynomial Regression (Degree 8)	0.74	2512.25
5-Layer Neural Network	0.12	14518.63

TABLE 5. Performance metrics for each prediction variable.

Output	R^2 score	MAE	RMSE
Supply	0.99	0.01v	0.0171v
PMOS width	0.977	25nm	33.43nm
NMOS width	0.977	10.6nm	14.26nm
Overall	0.98	11.37	20.96

$$R^2\ score = 1 - \frac{\sum (x_{predicted\ value} - x_{actual\ value})^2}{\sum (x_{actual\ value} - \bar{x})^2} \quad (3)$$

$$MAE = \frac{\sum |x_{actual} - x_{predicted\ value}|}{n} \quad (4)$$

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where, n represents the number of data points, $\bar{x}$ represents the mean value for the parameter x, x predicted value and x actual value represent the predicted and actual value of the parameter x, respectively. The results demonstrate that linear models achieved better performance in terms of R2 score and MSE, with significant computational efficiency and interpretability of predicted parameters. This performance alignment with linear models suggests that the targeted physical relationships between transistor widths and performance constraints exhibit linear characteristics within the operational space. The linear relationships between the shared input features and all target variables motivated the use of multi-target linear regression model for this study, capturing their underlying interdependencies. Grid searches is used to optimize regularization parameters and architectural choices. The selected hyper parameters represent the optimal configuration identified through this exhaustive search process, ensuring generalizability. The multi-output regressor achieved an overall R2 score of 0.984, a MAE of 11.37.

IV. EXPERIMENTAL RESULTS

The trained model is finally tested for the test data. For evaluating the model performance, R2 score, MAE and RMSE metrics are obtained for each predicted variable. RMSE is described in equation (5).

$$RMSE = \sqrt{\frac{\sum \left(x_{actual} - x_{predicted\ value}\right)^2}{n}} \qquad (5)$$

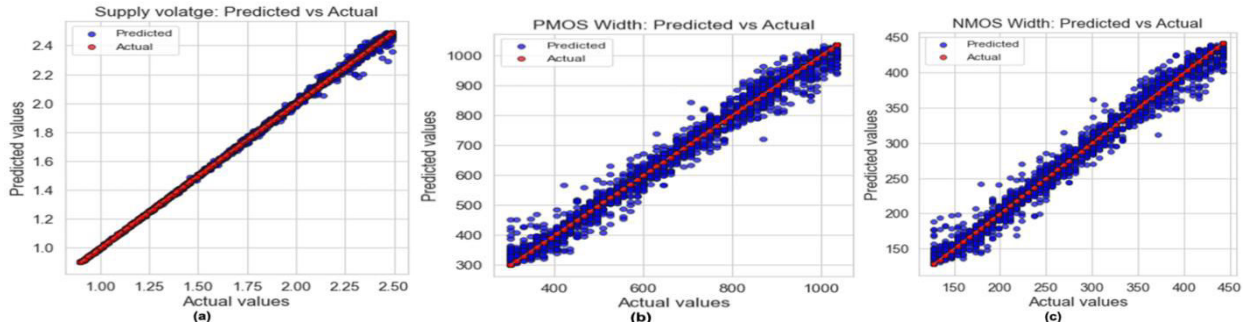


FIGURE.9. Performance of the ML model in terms of predicted and actual value of (a) Supply voltage (b) PMOS width (c) NMOS width.

The metric values for each variable are presented in Table 5. The performance of the ML model is analyzed by plotting the plots between the predicted values and the actual values in Figure 9 for supply voltage and NMOS/PMOS widths. These graphs demonstrate that the proposed multi-target regression model achieves accurate and well-behaved predictions across

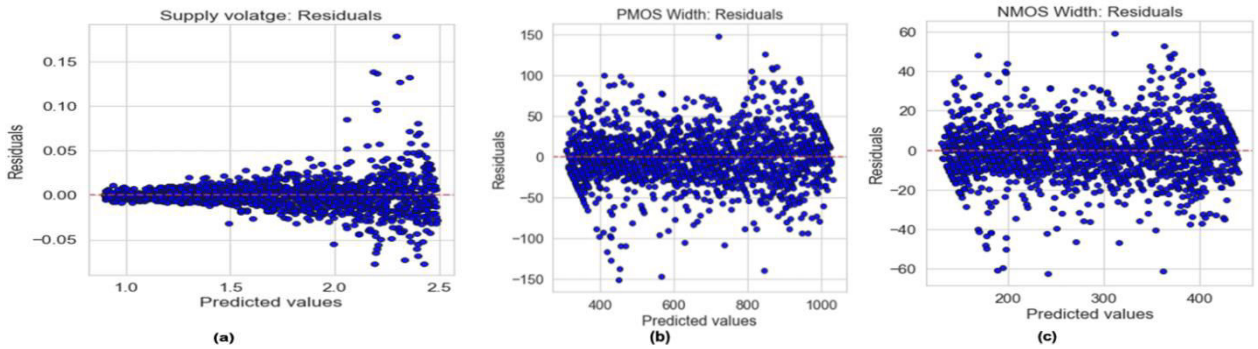


FIGURE.10. Performance of the ML model in terms of predicted and actual value of (a) Supply voltage (b) PMOS width (c) NMOS width.

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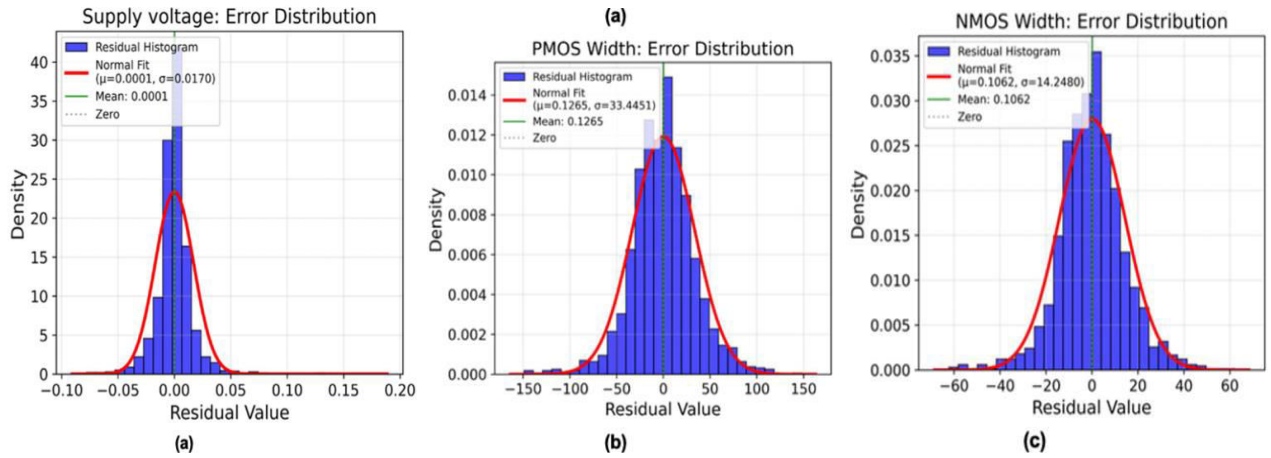


FIGURE.11.Error distribution of the multi-target regression model for (a) Supply voltage (b) PMOS width (c) NMOS width

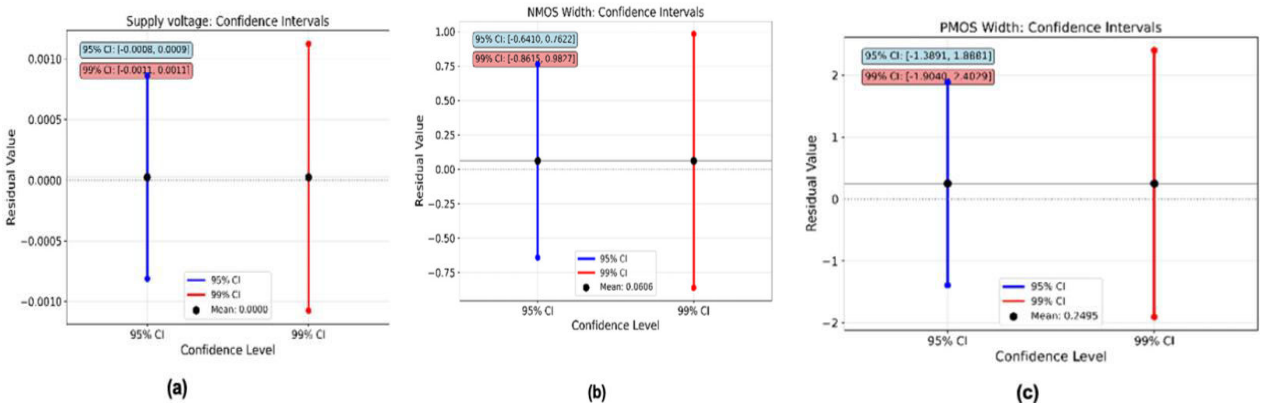


FIGURE.12. Confidence interval of the multi-target regression model for (a) Supply voltage (b) PMOS width (c) NMOS width

between actual and predicted values, generally referred to as prediction errors. Ideally, the residuals must be randomly scattered around the horizontal axis without following any discernible pattern which indicates that the model predictions are unbiased and well-fitted to the data. The residual plots in Figure 10 exhibits approximately symmetric, unimodal distributions centered near zero, which is consistent with a low-bias regression model for all output parameters. As most residuals are concentrated within a narrow band with scarcity of extreme outliers, it implies that the error variance is controlled, supporting the reliability of the model. In the case of supply voltage, the residuals are observed to be closely clustered around the zero-axis line, indicating smaller errors and better predictions compared to PMOS and NMOS widths.Similar patterns for all parameters ensure that the model can be used for concurrent prediction of these parameters without one target degrading the overall performance or introducing strong inter-target error correlations. Error prediction graphs for the trained model are shown in Figure 11 for supply voltage and NMOS and PMOS device dimension. The error distribution curves of supply voltage, NMOS width and PMOS width predictions exhibit approximately unimodal and symmetric shape, with residuals concentrated around zero and gradually tapering off toward both tails. These graphs not just establish the unbiased performance of the trained model and its accuracy but also help in identifying the failure of the model due to under/over predictions. In the case of supply voltage prediction, shown in Figure 11(a), the narrow, sharply peaked distribution of error shows that the model predicts supply voltage with high precision and negligible bias, so that almost all errors lie in a very small interval, making this target particularly reliable for downstream circuit level analysis and optimization. Small mean residual of $\mu \approx 0.1062$ and ≈ 0.1265 for NMOS and PMOS width predictions in Figure 11(b) and (c) respectively indicate that the

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multi-target regression model is unbiased in predicting these parameters with only a few samples in the extreme tails. Though most prediction errors fall within ±2σ roughly for both devices, the trained model is acceptable for robust circuit-parameter prediction. The 95% and 99%confidenceintervals of the residual parameter of the three target quantities are shown in Figure 12. The error distribution and confidence intervals for PMOS width show that the multi target model exhibits a larger spread of errors for PMOS than for NMOS, implying that PMOS sizing is some what harder to predict with few extreme outliers. The graphs for supply voltage prediction indicate that the multi target model's supply voltage error remains tightly controlled with negligible bias and high certainty in the voltage predictions. Thus, the multi-target model is seen to be accurate and unbiased enough for design-space exploration without the need to use separate single-target regressors.

V.CONCLUSION

A dataset comprising 8000 data points from simulation samples of a 3-bit Ripple Carry Adder was generated using NGSPICE to analyze the relationship between average power, worst-case delay, NMOS width, PMOS width, and supply voltage. By capturing and addressing the interdependencies between these parameters, the multi-target regression approach is chosen for training and testing the prediction model. The multi-output nature of the model enables it to efficiently utilize common information across targets, resulting in improved prediction accuracy and consistency. 80% of the dataset is used for training, the model that demonstrates an overall R2 score of 0.984, RMSE of 20.96 and a MAE of 11.37 for the 20% test data. These evaluation metrics are significant indicators of model's accuracy and reliability for predicting key parameters such as PMOS width, NMOS width, and supply voltage, based on desired power and delay constraints. These results demonstrate that the proposed regression approach can serve as a data-driven aid for early stage full-custom VLSI design, allowing faster estimation of transistor sizing and voltage conditions before detailed circuit-level simulations. Using this foundational study, the future works will embed predictive modelling within the VLSI design process to improve productivity and power efficiency of low-power digital circuits.

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